WHAT IS CLAIMED IS:

1. A display panel driver for driving a display panel in which capacitive light emitting cells serving as pixels are formed at intersections between a plurality of row electrodes serving as display lines and a plurality of column electrodes intersecting with said row electrodes in accordance with pixel data for the pixels based on an input video signal, the display panel driver comprising:

a pixel data pulse generation circuit which generates pixel data pulses by connecting said column electrodes and a power source line in accordance with said pixel data to apply said pixel data pulses to said column electrodes;

a resonance pulse power circuit which generates a resonance pulse power source voltage to apply said resonance pulse power source voltage to said power source line, said resonance pulse power circuit changing the resonance amplitude of said resonance pulse power source voltage while keeping a maximum voltage of said resonance pulse power source voltage in accordance with a pattern of a pulse sequence of said pixel data pulses;

a power prediction circuit which determines a predicted power consumption of said resonance pulse power circuit based on said pixel data for one field; and

a power consumption control circuit which controls said pixel data pulse generation circuit so as to adjust the power consumption of said resonance pulse power circuit in accordance with said predicted power consumption.

2. The display panel driver in accordance with claim 1, wherein said power prediction circuit determines, as said predicted power consumption, the root mean square of the resonance driving power when said resonance pulse power circuit is in resonance operation and the DC driving power when said resonance pulse power circuit is in DC operation.

3. The display panel driver in accordance with claim 1, wherein said power consumption control circuit controls said pixel data pulse generation circuit such that the number of times said pixel data pulses are applied within one field period is changed in accordance with said predicted power consumption.

4. The display panel driver in accordance with claim 1, wherein said power consumption control circuit controls said pixel data pulse generation circuit such that the number of pixel data pulses that are applied is smaller when said predicted consumption power is large than when said predicted consumption power is small.

5. The display panel driver in accordance with claim 1, wherein said pixel data pulse generation circuit is divided into a plurality of IC chips respectively corresponding to column electrode groups that are made of a predetermined number of column electrodes;

said power prediction circuit determines said predicted power consumption individually for each of said IC chips; and

said power consumption control circuit controls the

number of times that the pixel data pulses are applied within one field period individually for each of said IC chips based on said predicted power consumption for each of the chips.

6. The display panel driver in accordance with claim 5, wherein said power consumption control circuit performs the control such that the number of pixel data pulses that are applied is reduced only for those pixel data pulse generation circuits in which said predicted power consumption is large.

7. The display panel driver in accordance with claim 1, wherein, if at least two consecutive pixel data pulses that are applied to one of the row electrodes have the same voltage, then said resonance pulse power circuit reduces said resonance amplitude while sustaining said maximum voltage.

8. The display panel driver in accordance with claim 1, wherein said resonance pulse power circuit comprises:

a capacitor, one end of which is connected to ground;

a first current path made of a first switching element and a first coil that are arranged in series between the other end of said capacitor and said power source line;

a second current path made of a second switching element and a second coil that are arranged in series between the other end of said capacitor and said power source line;

a DC power source for generating said maximum voltage; and

a third switching element provided between the DC power source and said power source line;

and wherein said pixel data pulse generation circuit comprises:

a plurality of fourth switching elements which provide a connection between said power source line and said column electrodes in response to the logic level of said pixel data; and

a plurality of fifth switching elements which connect said column electrodes to ground in response to an inverted value of the logic level of said pixel data.

9. The display panel driver in accordance with claim 1, wherein said resonance pulse power circuit comprises drive control means that periodically repeat a control in which first only said first switching element is set to the ON state, then only said third switching element is set to the ON state, and then only said second switching element is set to the ON state.

10. A display panel driver for driving a display panel in which capacitive light emitting cells serving as pixels are formed at intersections between a plurality of row electrodes serving as display lines and a plurality of column electrodes intersecting with said row electrodes in accordance with pixel data for the pixels based on an input video signal, the display panel driver comprising:

a pixel data pulse generation circuit which generates pixel data pulses by connecting said column electrodes and a power source line in accordance with said pixel data to apply said pixel data pulses to said column electrodes;

a resonance pulse power circuit which generates a resonance pulse power source voltage to apply said resonance pulse power source voltage to said power source line, said resonance pulse power circuit changing the resonance amplitude of said resonance pulse power source voltage while keeping a maximum voltage of said resonance pulse power source voltage in accordance with a pattern of a pulse sequence of said pixel data pulses;

a power prediction circuit which determines a predicted power consumption of the resonance pulse power circuit based on said pixel data for one field; and

a power consumption control circuit which controls said pixel data pulse generation circuit so as to adjust the power consumption of said resonance pulse power circuit in accordance with said predicted power consumption;

wherein said pixel data pulse generation circuit is divided into a plurality of IC chips respectively corresponding to column electrode groups that are made of a predetermined number of column electrodes; and

wherein said IC chips are mounted on a plurality of flexible wiring boards that are respectively connected to said power source line and the column electrodes in said resonance pulse power circuit formed on the substrate of

the display panel.